

Cisco routers have **two types of queues**: a **hardware queue** and a **software queue**. The hardware queue, which is sometimes referred to as the transmit queue (TxQ), always uses FIFO queuing, and only when the **hardware queue is full** does the software queue handle packets.

Therefore, your queuing configuration only takes effect during periods of **interface congestion**, when the hardware queue has overflowed.

Congestion must occur on the interface first, which causes packets to be held in the TX Ring/TX Queue. When the TX Ring/TX Queue fills, IOS enables the queuing function on the interface.

Also note queues only form on **subinterfaces** when traffic shaping is enabled on the subinterface.

The **show controllers** command lists output that includes the output line that reads something like "tx\_limited=0(16)." The first number is 0 or 1, with 0 meaning that the statically-configured value is being used, and the number in parenthesis representing the length of the TX Ring/TX Queue. If the first number is 1, the TX Ring/ TX Queue has been automatically shortened by the IOS as a result of having a queuing tool enabled on the interface.

```
M1T-T3+ pa: show controller:
PAS unit 0, subunit 0, f/w version 3-93, rev ID 0x2800001, version 3
idb = 0x64029F9C, ds = 0x6402B744, ssb=0x6402BAF8
Clock mux=0x30, ucmd_ctrl=0x0, port_status=0x1
Serial config=0x8, line config=0x1B0202
maxdgram=4500, bufpool=128Kb, 256 particles

    rxLOS inactive, rxLOF inactive, rxAIS inactive
    txAIS inactive, rxRAI inactive, txRAI inactive
line state: up
cable type : T3  cable, received clockrate 44201430

base0 registers=0x3C800000, base1 registers=0x3C802000
mxt_ds=0x64E3336C, rx ring entries=124, tx ring entries=254
statring=0xE329A00, statr shadow=0x6402D838, stat_head=37
rxring=0xE3297C0, rxr shadow=0x6402D20C, rx_head=10
txring=0xE32A040, txr shadow=0x6402E464, tx_head=220, tx_tail=220, tx_count=0
throttled=0, enabled=0
halted=0, last halt reason=0
Microcode fatal errors=0
rx_no_eop_err=0, rx_no_stp_err=0, rx_no_eop_stp_err=0
rx_no_buf=0, rx_soft_ouerrun_err=180, dump_err= 0, bogus=0, mxt_flags=0x2C
tx_ouerrun_err=0, tx_soft_ouerrun_err=0, tx_limited=0(256)
tx_fullring=42125, tx_started=199254890, mxt_flush_count=0
rx_int_count=809850178, tx_int_count=509718014
```

Q. Can the Layer 3 (L3) Catalyst switches **mark or rewrite** IP precedence Type of Service (ToS) bits in an IP packet?

A. No, but they do honor them and use them for input classification and output scheduling.